Xylon d.o.o.

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Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Contact Xylon
Reference Designs & Application Notes	Contact Xylon
Additional Items	Linux OS SW driver, bare-metal
Simulation Tool Used	
ModelTech's Modelsim	
Support	
Support provided by Xylon	

Features

- Supports Xilinx® Zynq™-7000 AP SoC and all Xilinx FPGA families
- Converts camera sensor video from Bayer color space to RGB or YCrCb 4:2:2
- Input resolution up to 4096x4096 (including 4K2K)
- Supports all possible Bayer pattern combinations (first two pixels: BG, RG, GB, GR)
- Supports different input interface standards:
  - Parallel - data, control and clock signals
  - AXI4-Stream - AXI4 compliant video interface
  - LVDS - 1:12 deserialization with embedded clock
- Supports different output interface standards:
  - Parallel - data, control and clock signals
  - AXI4-Stream - AXI4 Compliant video interface
  - Memory - XMB, PLBv46, NPI or AXI4
- Cropping two pixels or two lines from each side of the input image
- RGB (24-bit RGB888 or 32-bit ARGB8888) or YCrCb (16-bit 4:2:2) output color representation
- Configurable pixel row stride (512, 1024, 2048, 4096)
- Prepared for Xilinx Vivado® Design Suite and Xilinx Platform Studio (XPS) implementation tools
- IP core configurable through generic parameters or register interface (PLBv46 or AXI4-Lite)

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)			LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	vclk	rclk									
Spartan®-6 (XC6SLX75T-3)	180	180	220	2381	372 (908/930)	12	0	6	0	0	0	ISE® 14.6
Virtex®-6 (XC6VLX75T-3)	200	180	220	2535	396 (907/928)	12	0	6	0	0	0	ISE® 14.6
Kintex®-7 (XCK325T-3)	200	180	220	2637	412 (909/920)	12	0	6	0	0	0	ISE® 14.6

Notes:
1) Assuming the following configuration: parallel input, 64-bit AXI4 memory interface, no cropping, no scaling, AX4-Lite register interface
2) Assuming only video inputs are routed off-chip, memory and register interfaces are connected internally
3) Implementation statistics given for Artix-7 and Kintex-7 FPGAs are also valid for the Zynq-7000 AP SoC family

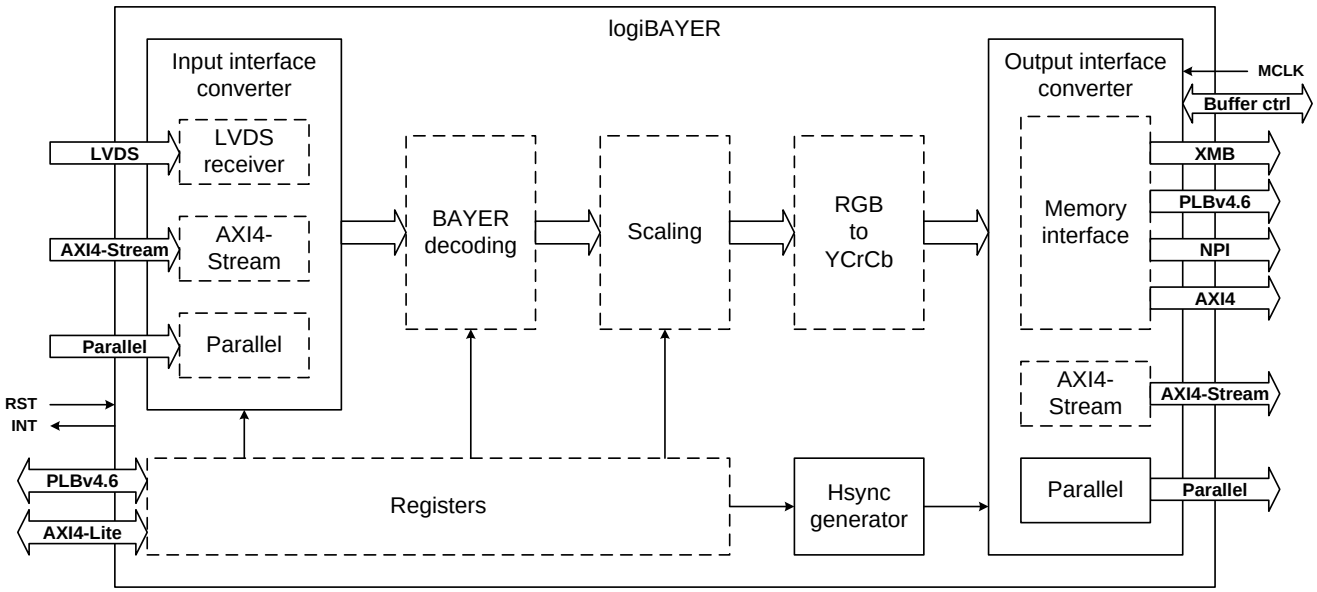

Figure 1: logiBAYER Architecture

Features (cont)

- Flicker-free video output assured by double or triple buffering on memory output interface
- Scaling down two times vertically and two times horizontally
- Parametrical VHDL design that allows tuning of slice consumption and features set
- Simple Plug'n'Play with Xilinx, third-party and Xylon logicBRICKS IP cores, such as:
  - logiMEM Flexible Memory Controller
  - logiCVC-ML Compact Multilayer Video Controller
  - logiWIN Versatile Video Input
  - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
  - logiBMP Bitmap 2.5D Graphics Accelerator

Applications

- Automotive Driver Assistance Systems (ADAS): Surround View, Lane Departure Warning, Front- and Rear-View camera, others
- Industrial systems: Surveillance, Pipe Inspection, Test & Measurement, others
- Defense and Aerospace video camera based systems…

General Description

The logiBAYER is an IP core from the Xylon logicBRICKS IP core library, optimized for Xilinx All Programmable SoCs and FPGAs and designed for real-time Bayer pattern demosaicing (decoding). The most common single-chip cameras use Bayer pattern sensors, which have specific physical pixel positions and assign a single color value (Red, Green, or Blue) to each pixel. This Bayer encoding (mosaicing) enables approximation of the other two primary colors using surrounding pixels, for all sensor pixels.

The logiBAYER IP core converts input camera sensor video from the Bayer coded color space into the RGB or YCrCb color space. It supports all possible Bayer pattern combinations (see Figure 3). The color space conversion includes real-time approximations of missing primary colors and generation of the RGB (24-bit RGB888 or 32-bit ARGB8888) or YCrCb (16-bit 4:2:2) video output. The core can be used as an input into a camera processor IP chain designed by Xylon logicBRICKS IP cores, Xilinx and third-party IP cores.

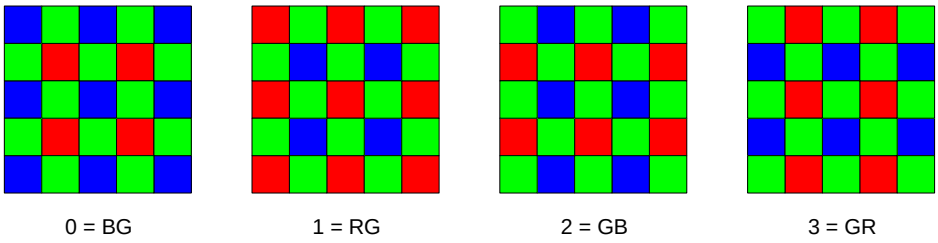

Figure 2: Bayer Pattern Combinations: BG, RG, GB and GR

The logiBAYER IP core consumes modest programmable logic resources, and multiple logiBAYER IP cores can simultaneously process video inputs from multiple cameras in a single low-cost FPGA. Advanced Automotive Driver Assistance Systems (ADAS) are illustrative examples of multi-camera applications: http://www.logicbricks.com/Solutions/Surround-View-DA-System.aspx

logiBAYER IP core is highly configurable and users can setup its configuration prior to the FPGA implementation. The IP includes different video input and output standards including a built-in LVDS receiver compatible to, i.e. Aptina MT9V022/023 CMOS image sensors.

The logiBAYER IP core supports camera resolutions up to 4096x4096 (4K2K resolution supported) and supports input synchronization signals (vertical sync and data enable) with an arbitrary polarity. The processed video (RGB or YCrCb) can be passed through the streaming video interface (low-latency) to other IPs for further video processing, or stored for post-processing into frame buffers implemented in an external memory. The IP core supports an optional image scaling of 2x vertically and 2x horizontally with VHDL generics. The IP core's configuration can be completely defined with generic parameters but logiBAYER also supports some parameters to be defined through configuration registers controlled through CPU interface (PLB or AXI4-Lite).

Figure 3 shows a block schematic of an FPGA-based Automotive Surround View system utilizing four instances of the logiBAYER IP core that decodes four Bayer encoded video streams from video cameras.

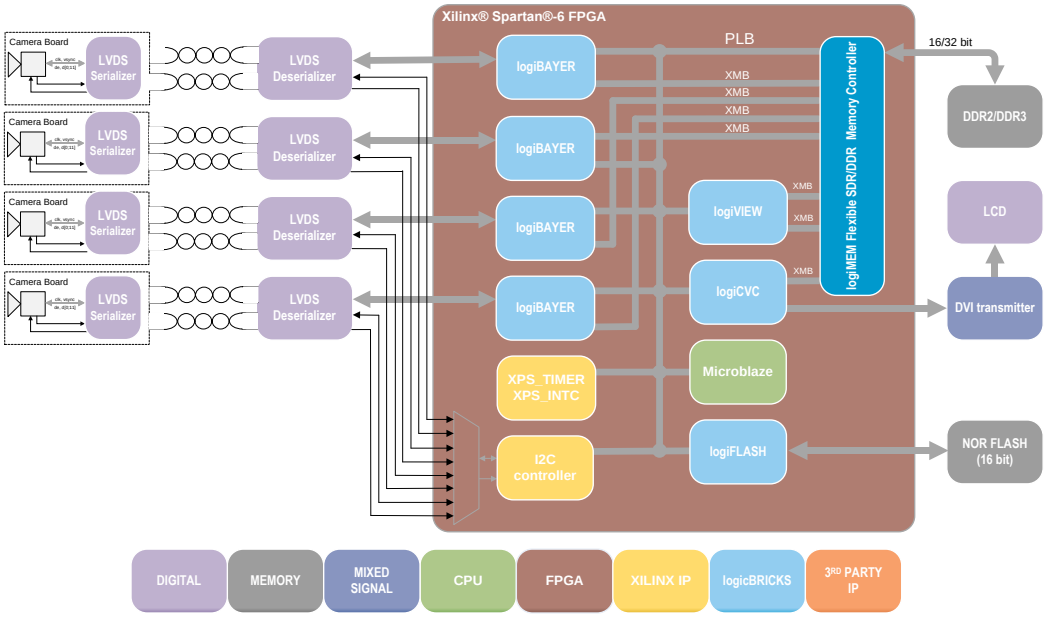

Figure 3: An Example FPGA Architecture – 4x logiBAYER in Automotive Surround View System

Functional Description

The Figure 1 presents internal logiBAYER IP core's architecture. The logiBAYER functional blocks are: Input interface converter, Bayer decoding module, Scaling module, RGB to YCrCb converter, Output interface converter, Registers and Hsync generator.

Input interface converter

logiBAYER supports three different input interfaces:

- Parallel - 8-bit data, de, vsync and clock signal
- AXI4-Stream - AXI4 Compliant video type interface
- LVDS - One signal pair with 12:1 data serialization with embedded clock

The parallel interface supports sampling on both clock edges. Control signals' (vsync, de) polarity can be changed through generic parameters.

The AXI4-Stream input interface is AMBA AXI4 standard compliant and can be used with any type of AXI4 compliant video source peripheral.

Bayer decoding

Bayer decoding algorithm uses 5 horizontal lines of input video image. 4 lines stored in the input line buffer are combined with the incoming 5th line and setup in correct order for Bayer decoding filter. The filter sub-block calculates R, G and B values from surrounding pixels and executes additional corrections of the output stream.

The output image from the Bayer decoder can be either cropped (two pixels from left or right, or two lines from top or bottom), or supplied with the calculated marginal pixels (no cropping).

Scaling module

An optional image 2x vertical and horizontal can be enabled by C_SCALING generic parameter. Furthermore, an optional registers block enables real time scaling on/off control.

RGB to YCrCb converter

Bayer decoded output RGB pixels can be optionally converted to YCrCb color space. This color space converter converts 24-bit RGB pixels into 16-bit YCbCr 4:2:2 pixels. The 8-bit luminance (Y) value is provided for every output pixel, but the 8-bit chroma (Cr and Cb) values are shared by two horizontally neighboring pixels.

Output interface converter

logiBAYER supports three different output interfaces:

- Parallel - 24-bit data, de, vsync and clock signal
- AXI4-Stream - AXI4 Compliant video type interface
- Memory - XMB, PLBv46, NPI or AXI4

The AXI4-Stream and all configurable memory interfaces support RGB (24-bit RGB888 or 32-bit ARGB8888) or YCrCb (16-bit 4:2:2) outputs. The parallel interface supports RGB (24-bit RGB888) or YCrCb (16-bit 4:2:2) outputs.

Control signals' (vsync, de) polarity can be changed by generic parameters.

The memory interface between Bayer decoding block and an external memory (SDR, DDR, …) consists of a FIFO, memory addresses generator, and control signals generator.

Registers

An optional registers field can be used in applications that support changeable video inputs resolutions, scaling modes, etc. In applications that use fixed video processing setup, the logiBAYER IP core can be configured without registers and save programmable logic resources.

Hsync generator

Majority of video frame grabbers (including Xylon's logiWIN Versatile Video Input IP core) require horizontal synchronization (hsync) control signal, which is usually not generated by camera sensors. The logiBAYER IP core solves that interfacing issue with Hsync generator module that generates the hsync signal from other video control signals.

Core Modifications

The core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator and Xilinx Platform Studio implementation tools. Many logiBAYER configuration parameters are selectable prior to VHDL synthesis, and the following table presents a subset of available parameters.

Table 2: Subset of logiBAYER VHDL configuration parameters

Parameter	Description
C_INPUT_INTERFACE	Input interface selection: 0 - Parallel, 1 - AXI4-Stream, 2 - LVDS
C_OUTPUT_INTERFACE	Output interface selection: 0 - Parallel, 1 - AXI4-Stream, 2 - Memory
C_REGS_INTERFACE	Interface to registers: 0 - No registers, 1 - PLBv4.6 Slave, 2 - AXI4-Lite
C_VMEM_INTERFACE	Interface to video memory: 0 - XMB, 1 - PLBv4.6, 2 - NPI, 3 - AXI4
C_FIRST_TWO_PIX	First two pixels in Bayer pattern: 0 - Blue Green (BG), 1 - Red Green (RG), 2 - Green Blue (GB), 3 - Green Red (GR)
C_CROP_LEFT_X	Crop image left edge: 0 - keep original resolution, 1 - crop two pixels from left side of the image
C_CROP_RIGHT_X	Crop image right edge: 0 - keep original resolution, 1 - crop two pixels from right side of the image
C_CROP_UP_Y	Crop image top edge: 0 - keep original resolution, 1 - crop two lines from top side of the image
C_CROP_DOWN_Y	Crop image bottom edge: 0 - keep original resolution, 1 - crop two lines from bottom side of the image
C_SCALING	Enable image scaling: 0 - no scaling, 1 - enable two times scaling
C_RGB2YCRCB	YCrCb output (instead of RGB): 0 - No, 1 - Yes

The logiBAYER is designed with regards to adaptability to various cameras. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiBAYER core or to supplement some of your specific functions, you can allow us to tailor the logiBAYER to your requirements.

Core I/O Signals

The core signals I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous reset; high active
Parallel Input Interface		
VCLK_IN	Input	Parallel pixel clock input
VSYNC_IN	Input	Parallel vertical synchronization input
DE_IN	Input	Parallel data enable input
CE_IN	Input	Parallel clock enable input
DATA_IN(7:0)	Input	Parallel bayer data input
AXI4-Stream Input Interface		
S_AXIS_VIDEO_ARESETN	Input	Slave AXI4-Stream - reset
S_AXIS_VIDEO_ACLK	Input	Slave AXI4-Stream - clock
S_AXIS_VIDEO_TDATA(7:0)	Input	Slave AXI4-Stream - pixel data
S_AXIS_VIDEO_TVALID	Input	Slave AXI4-Stream - pixel data valid
S_AXIS_VIDEO_TREADY	Output	Slave AXI4-Stream - slave ready
S_AXIS_VIDEO_TUSER(0:0)	Input	Slave AXI4-Stream - start of frame
S_AXIS_VIDEO_TLAST	Input	Slave AXI4-Stream - end of line
LVDS Input Interface		
LVDS_CLK	Input	LVDS deserializer clock = 12*pixel clock
LVDS_CLK90	Input	LVDS deserializer clock = 12*pixclk, phase shifted 90 degrees
LVDS_DATA_P	Input	LVDS input data pair – positive
LVDS_DATA_N	Input	LVDS input data pair – negative
LVDS_PIX_CLK_IN	Input	LVDS parallel pixel clock input. Valid only when fixed pix_clk period is used
Parallel Output Interface		
VCLK_OUT	Output	Parallel pixel clock output
VSYNC_OUT	Output	Parallel vertical synchronization output
HSYNC_OUT	Output	Parallel horizontal synchronization output
DE_OUT	Output	Parallel data enable output
DATA_OUT(23:0)	Output	Parallel data output
AXI4-Stream Output Interface		
M_AXIS_VIDEO_ARESETN	Input	Master AXI4-Stream - reset
M_AXIS_VIDEO_ACLK	Input	Master AXI4-Stream - clock
M_AXIS_VIDEO_TDATA(32:0)	Output	Master AXI4-Stream - pixel data
M_AXIS_VIDEO_TVALID	Output	Master AXI4-Stream - pixel data valid
M_AXIS_VIDEO_TREADY	Input	Master AXI4-Stream - slave ready
M_AXIS_VIDEO_TUSER(0:0)	Output	Master AXI4-Stream - start of frame
M_AXIS_VIDEO_TLAST	Output	Master AXI4-Stream - end of line
Memory Output Interface		
MCLK	Input	Memory clock input - used for all supported memory interfaces
XMB Interface	Bus	Xylon Memory Bus. Refer to Xylon logiMEM User's Manual
PLBV46 Master Interface	Bus	Refer to Xilinx-IBM Core connect specification
NPI Interface	Bus	Refer to Xilinx MPMC (Multi Port Memory Controller) specification
AXI4 Master Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Register Interface		
PLBv46 Slave Interface	Bus	Refer to Xilinx-IBM Core connect specification
AXI4-Lite Slave Interface	Bus	Refer to AMBA AXI version 4 specification from ARM

Signal	Signal Direction	Description
Auxiliary Signals		
CURR_VBUFF(1:0)	Output	Triple buffering - current video memory buffer
NEXT_VBUFF(1:0)	Input	Triple buffering - next video memory buffer to write to
SW_VBUFF_REQ	Output	Triple buffering - request for buffer switching
SW_VBUFF_GRANT	Input	Triple buffering - buffer switching granted
INTERRUPT	Output	Interrupt signal - level sensitive, high active

Verification Methods

logiBAYER is fully supported by the Xilinx Vivado IP Integrator and Platform Studio integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiBAYER implementation does not require any particular skills beyond general Xilinx tools knowledge. The encrypted IP is shipped with compiled simulation libraries for ModelSim.

The logiBAYER evaluation IP core can be downloaded from Xylon web site and be fully evaluated in hardware:

URL: http://www.logicbricks.com/Products/logiBAYER.aspx

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

Xylon logiBAYER IP core can be evaluated on any Xilinx Zynq-7000 AP SoC or FPGA based evaluation platform that supports the video input functionality.

The logiBAYER IP core is often used with the logiVIEW Perspective Transformation and Lens Correction Image Processor IP core for video and imaging applications. The logiVIEW IP core removes fish eye distortions caused by extreme wide-angle Field Of View (FOV) lenses, makes complex homographic transformations and non-homographic transformations, i.e. video texturing on curved surfaces.

To learn more about the Xylon logiVIEW IP core, contact Xylon or visit the web:

Email: support@logicbricks.com
URL: http://www.logicbricks.com/Products/logiVIEW.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please visit our web shop or contact Xylon for pricing and additional information:

Email: sales@logicbricks.com
URL: www.logicbricks.com

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Revision History

Version	Date	Note
2.01.	06.03.2009.	Initial Xylon release – new doc template
3.00.	26.10.2009.	Updated for new logiBAYER features
3.02	19.04.2010.	Bugs fixed and horizontal sync generator added
6.00	20.04.2012.	Input/output interface modules, AXI4-Lite support, AXI4-Stream support, AXI4 interface support,
6.01	16.06.2013.	Small change in AXI4-Stream signal naming
6.02.	01.10.2013	Version updated according to IP core
6.03.	02.12.2013.	Increased maximal resolution to 4096x4096, Independent crop support for left, right, up and down